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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,228	11/29/2001	Daniel M. Joffe	72129	2539

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 06/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/997,228	JOFFE ET AL.
	Examiner	Art Unit
	Walter F Briney III	2644

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Navabi et al. (US Patent 5,585,763).

Claim 1 is limited to **a synthetic impedance driver circuit for driving a load**. Navabi discloses a controlled impedance amplifier (i.e. **a synthetic impedance driver circuit for driving a load**) (abstract). Navabi discloses **an input port** (figure 2, element 325) **adapted to receive an input signal** (figure 2, element i_{in}) **to be coupled to said load** (figure 2, element R_L). Navabi discloses **an output port** (figure 2, element 360) **adapted to apply an output signal** (figure 2, element V_{out}) **to said load** (figure 2, element R_L). Navabi discloses **an operational amplifier** (figure 2, element 310) **having an input** (figure 2, positive terminal of 310) **coupled to said input port** (figure 2, element 325) **and an output**. Navabi discloses that the operational amplifier drives output amplifiers 347 and 357 (i.e. **coupled to said output port**) and drives feedback transistors 345 and 351 (i.e. **over a circuit path through which an output impedance of said driver circuit is synthesized**). The feedback resistor R_f is not a part of the output or transistor feedback path (i.e. **said circuit path being exclusive of one or more series coupled electrical energy-dissipative elements**). Thus, Navabi

inherently discloses **that said synthesized output impedance of said driver circuit is defined essentially exclusive of series-coupled electrical energy-dissipative elements**. Therefore, Navabi anticipates all limitations of the claim.

Claim 2 is limited to **the synthetic impedance driver circuit according to claim 1**, as covered by Navabi. Navabi discloses **an output voltage feedback resistor** (figure 2, element R_f) **coupled between said output port and an input of said operational amplifier circuit**. Navabi also discloses **a current sensing circuit** (figure 2, element 345 and 355) **coupled between said output port and an input of said operational amplifier**. These transistors are connected as feedback at the x-intersection of lines 343, 353, and 325. Because transistors 345 and 355 are identical to the output transistors 347 and 357 and are driven by the same control circuit they feedback a replica of the output current (i.e. **and being operative to feed back a current representative of output current applied to said output port**). The feedback inherently creates synthesized **output impedance defined in accordance with said feed back current**. Therefore, Navabi anticipates all limitations of the claim.

Claim 3 is limited to **the synthetic impedance driver circuit according to claim 2**, as covered by Navabi. As seen in figure 2, the feedback is an output of current mirror transistors 345 and 355 (i.e. **wherein said current sensing circuit comprises a current mirror circuit**). Therefore, Navabi anticipates all limitations of the claim.

Claim 4 is limited to **the synthetic impedance driver circuit according to claim 2**, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs a level-shifting function with two outputs (figure 2, elements

315, 320). Navabi discloses **an output coupling circuit** (figure 2, elements 345, 355, 347, 357) **having an input coupled to said output of said operational amplifier and level-shifted outputs**. Navabi discloses complementary output transistors 347 and 357 that are **respectively coupled between said level-shifted outputs of said output coupling circuit and said output port**. Navabi discloses **complementary polarity current mirror transistor circuits** (figure 2, elements 345, 355) **respectively coupled between said complementary polarity output transistor circuits and an input of said operational amplifier**. Therefore, Navabi anticipates all limitations of the claim.

Claim 5 is limited to **the synthetic impedance driver circuit according to claim 4**, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs a level shift with a plurality of output levels (i.e. **wherein said output coupling circuit includes a level shifter**) (figure 2, element 315, 320). Therefore, Navabi anticipates all limitations of the claim.

Claim 6 is limited to **the synthetic impedance driver circuit according to claim 5**, as covered by Navabi. Navabi discloses an **operational amplifier that has a first polarity input** (figure 2, positive terminal of 310) **to which said input signal** (figure 2, element i_{in}) **and said output voltage feedback resistor are coupled** (figure 2, element R_f), **and a second polarity input** (figure 2, negative terminal of 310) **to which a reference voltage is coupled** (figure 2, element V_{cm}). Therefore, Navabi anticipates all limitations of the claim.

Claim 7 is limited to **the synthetic impedance driver circuit according to claim 6**, as covered by Navabi. Navabi discloses a x-intersection where lines 343, 353 and 325 cross (i.e. **wherein said complementary polarity current mirror circuits have a first common node coupled to said first polarity input of said operational amplifier**). Therefore, Navabi anticipates all limitations of the claim.

Claim 8 is limited to **the synthetic impedance driver circuit according to claim 7**, as covered by Navabi. Navabi discloses a x-intersection where lines 344, 352, and 360 cross (i.e. **wherein said complementary polarity output transistor circuits have a second common node coupled to said output port**). Therefore, Navabi anticipates all limitations of the claim.

Claim 9 is essentially the same as claim 6 and is rejected for the same reasons.

Claim 10 is limited to **the synthetic impedance driver circuit according to claim 2**, as covered by Navabi. Navabi discloses a second embodiment that adds a switching input to the operational amplifier (figure 8A). It is clear that this embodiment incorporates all the limitations of claim 2. In addition, Navabi discloses that **said operational amplifier circuit** (figure 8A, element 910) **has a first polarity input** (figure 8A, IN1+ terminal of 910) **to which said input signal is coupled** (figure 8A, i_{in})**, and a second polarity input** (figure 8A, IN2+ terminal of 910) **to which said output voltage feedback resistor and said feed back current are coupled**. Therefore, Navabi anticipates all limitations of the claim.

Claim 11 is limited to **a synthetic impedance driver circuit**. Navabi discloses a controlled impedance amplifier (i.e. **a synthetic impedance driver circuit**) (abstract).

Navabi discloses **an operational amplifier** (figure 2, element 310) **having a first input** (figure 2, positive terminal of 310) **coupled to receive an input signal** (figure 2, element i_{in}), **a second input** (figure 2, negative terminal of 310) **coupled to a reference voltage** (figure 2, element V_{cm}), **and a voltage feedback resistor** (figure 2, element R_f) **coupled between an output port and an input of said amplifier**. Navabi discloses **an output current-dependent current source** (figure 2, elements 345, 355). These devices are biased by devices 346 and 356 to inherently supply **a prescribed fraction k of output current at said output port over a current feedback path to an input of said operational amplifier**. Because all elements are disclosed by Navabi, Navabi inherently discloses **that the output impedance of said synthetic impedance driver circuit is synthesized in terms of the mirror current ratio k and the value of said output voltage feedback resistor**. Therefore, Navabi anticipates all limitations of the claim.

Claim 12 is limited to **the synthetic impedance driver circuit according to claim 11**, as covered by Navabi. Navabi discloses that the operational amplifier (figure 2, element 310) has a feedback path through devices 345 and 355, and that the **output** is generated by elements 347 and 357, therefore, **no energy dissipative devices** are present in the output. Also, the current feedback by elements 345 and 355 **is free of dissipative elements**. Therefore, Navabi anticipates all limitations of the claim.

Claim 13 is limited to **the synthetic impedance driver circuit according to claim 12**, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs level shifting to properly control all output transistors (i.e.

said output coupling circuit including a level shifter). The shifter has **a first** (figure 2, element 315) **and second** (figure 2, element 320) **level-shifted outputs, respectively coupled to first** (figure 2, element 347) **and second** (figure 2, element 357) **complementary polarity output transistors coupled to said output port, and associated complementary current mirror transistors** (figure 2, elements 345, 355) having **a node** at the intersection of lines 343, 353 and 325. Because 345 and 355 are further controlled by 346 and 356, they inherently provide **said prescribed fraction k of output current at said output port to an input of said operational amplifier**. Therefore, Navabi anticipates all limitations of the claim.

Claim 14 is limited to **the synthetic impedance driver circuit according to claim 12**, as covered by Navabi. Navabi discloses **an input signal** (figure 2, element i_{in}) **is coupled to a noninverting input** (figure 2, positive terminal of 310) **of said operational amplifier**. Therefore, Navabi anticipates all limitations of the claim.

Claim 15 is limited to **the synthetic impedance driver circuit according to claim 13**, as covered by Navabi. Navabi discloses a feedback path including several resistors (figure 8, elements Rf1, Rf2) coupled to a mirror current feedback (figure 8, elements output from 347 and 357). One of these resistors is the resistive feedback from the output. The other is **a first auxiliary resistor**. Navabi also discloses that a third resistor (i.e. **a second auxiliary resistor**) is used (column 8, lines 32-35). The resistors are shown as being feedback to **non-inverting reference inputs of the amplifier** (figure 8, element 910). Therefore, Navabi anticipates all limitations of the claim.

Claim 16 is limited to **the synthetic impedance driver circuit according to claim 13**, as covered by Navabi. Navabi discloses **a feedback operational amplifier** (figure 7, element 370) **having inputs respectively coupled to said output port** (figure 7, element 342) **and to said current mirror node** (figure 7, element 343 by way of 346 and 341), **and an output** (figure 7, seen coupled to 346) **coupled as a control input to a feedback transistor** (figure 7, element 346) **having its current flow path coupled to power supply terminals** (figure 7, element V_{dd} and Ground indicated by the inverted arrow) **for said driver circuit through a first auxiliary current mirror circuit** (figure 7, element 345A) **and a first auxiliary bias current source** (figure 7, element 355A). Navabi discloses that the feedback transistor (figure 7, element 346) is used in conjunction with a second feedback transistor (figure 7, element 356). They control the voltage at node 325. As such, they must track the output current and are inherently active to provide the correct scaled current to be feedback to the operational amplifier (i.e. **said first auxiliary bias current source maintaining said feedback transistor in a conductive state for both polarities of output current**). Navabi discloses **a second auxiliary current mirror circuit** (figure 7, element 345B) **coupled to said current mirror circuit and to the inverting input of said driver amplifier circuit, to which a second auxiliary bias current source** (figure 7, element 355B) **is coupled**. Therefore, Navabi anticipates all limitations of the claim.

Claims 17-19 are essentially the same as claims 1-3, respectively, and are rejected for the same reasons.

Claim 20 is essentially the same as claim 16 and is rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
5/27/04

MINSUN OH HARVEY
PRIMARY EXAMINER